CLAIMS

What is claimed is:

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1. A semiconductor workpiece, comprising

a metal layer;

an inorganic dielectric ARC layer disposed on the metal layer; and

a photoresist layer disposed on the ARC layer opposite the metal layer.

2. The workpiece recited in claim 1 wherein the ARC layer comprises silicon oxynitride.

3. The workpiece recited in claim 2 wherein the ARC layer consists essentially of silicon oxynitride.

4. The workpiece recited in claim 1 wherein the ARC layer has a substantially uniform thickness over topical non-planarities on the metal layer.

5. The workpiece recited in claim 4 wherein the ARC layer is deposited on the metal layer by chemical vapor deposition.

6. The workpiece recited in claim 5, wherein the ARC layer is deposited on the metal layer by plasma enhanced chemical vapor deposition.

7. The workpiece recited in claim 1 wherein the photoresist layer is between 0.1 to 2 microns thick.

8. The workpiece recited in claim 7 where in the photoresist layer is 0.6 to 1.0 microns thick.

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9. A metallic stack for a semiconductor interconnect, comprising:
a metal layer;
an inorganic dielectric ARC layer disposed on the metal layer; and
a barrier layer disposed on the metal layer opposite the arc layer.

10. The metallic stack recited in claim 9 wherein the ARC layer comprises silicon oxynitride.

11. The metallic stack recited in claim 10 wherein the ARC layer consists essentially of silicon oxynitride.

12. The metallic stack recited in claim 9 wherein the ARC layer has a substantially uniform thickness over topical non-planarities on the metal layer.

13. The metallic stack recited in claim 12 the ARC layer is deposited on the metal layer by chemical vapor deposition.

14. The metallic stack recited in claim 13 wherein the ARC layer is deposited on the metal layer by plasma enhanced chemical vapor deposition.

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15. The metallic stack recited in claim 9 wherein the stack is about 1,000 to 20,000 Amgstrans thick.

16. The metallic stack of claim 15 wherein the stack is about 5,000 to 8.000 Amgstrans thick.

17. A semiconductor device, comprising:

an oxide layer formed on a wafer; and

at least one microelectronic structure extending from the ovide layer and including:

a barrier layer disposed on the oxide layer;

a metal layer disposed on the barrier layer; and

an inorganic dielectric ARC layer disposed on the metal layer.

18. The semiconductor device recited in claim 17 wherein the at least one microelectronic structure further includes a residual photoresist layer disposed on the ARC layer.

19. The semiconductor device recited in claim 17 wherein the ARC layer consists essentially of silicon oxynitride.

20. The semiconductor device recited in claim 19 wherein the ARC layer is formed by plasma enhanced chemical vapor deposition.

claims 17-20 control as most comprehensive